Other variations of the FIG. **13** embodiment are possible. For example, floating guard-rings may be used on the outside of trench **1306***c* with or without field plate structure **1310**. Although cell trenches **1306***a,b* and termination trench **1306***c* are shown to be narrower than the cell trenches in FIG. **8**, trenches **1306***a,b,c* may be widened as in FIG. **8**. Further, the width Wt of termination trench **1306***c* may be designed to be different than cell that of trenches **1306***a,b* if desired.

FIG. **14** is a cross sectional view showing another termination structure in combination with the cell structure shown in FIG. **8**. As shown, the termination structure includes a termination trench **1408** lined with an insulation layer **1410** along its sidewalls and bottom. A field plate **1406** (e.g., from doped polysilicon) is provided over insulation layer **1410** in trench **1408**, and extends laterally over the surface and away from the active regions.

Although the above-described termination structures are shown in combination with the cell structure in FIG. **8**, these and other known termination structures may be combined with any of the cell structures described above.

While the above is a complete description of the embodiments of the present invention, it is possible to use various alternatives, modifications and equivalents. For example, the different embodiments described above are n-channel power MOSFETs. Designing equivalent p-channel MOSFETs would be obvious to one skilled in the art in light of the above teachings. Further, p+ regions, similar to p+ regions **210***a,b* in the FIG. **2** structure, may be added in the body regions of the other structures described herein to reduce the body resistance and prevent punch-through to the source. Also, the cross sectional views are intended for depiction of the various regions in the different structures and do not necessarily limit the layout or other structural aspects of the cell array. Therefore, the scope of the present invention should be determined not with reference to the above description but should, instead, be determined with reference to the appended claim, along with their full scope of equivalents.

What is claimed is:

1. A MOSFET comprising:

a first semiconductor region having a first surface;

a first trench region extending from the first surface into the first semiconductor region; and

a first plurality of floating regions along a sidewall of the first trench region, the first plurality of floating regions having a conductivity type opposite that of the first semiconductor region.

2. The MOSFET of claim **1** wherein the first plurality of floating regions are spaced along the outer sidewall of the first trench region such that a depletion region formed in the first semiconductor region during an operation mode of the MOSFET is extended into the first semiconductor region away from the first surface.

3. The MOSFET of claim **1** further comprising:

a body region extending from the first surface into the first semiconductor region, the body region being of a conductivity type opposite that of the first semiconductor region;

a source region in the body region, the source region being of the same conductivity type as the first semiconductor region;

a second trench region extending from the first surface into the first semiconductor region; and

a gate in the second trench region extending across a portion of the body region and overlapping the source and the first semiconductor regions such that a channel region extending perpendicularly to the first surface is formed in the body region between the source and first semiconductor regions.

4. The MOSFET of claim **1** further comprising:

first and second body regions each extending from the first surface into the first semiconductor region, the first body region being laterally spaced from the second body region to form a JFET region therebetween, the first and second body regions being of a conductivity type opposite that of the first semiconductor region; and

first and second source regions in the first and second body regions respectively, the first and second source regions being of the same conductivity type as the first semiconductor region.

5. The MOSFET of claim **4** further comprising a gate extending over but being insulated from the JFET region and a portion of the first and second body regions, and overlapping the first and second source regions such that a channel region is formed along a body surface of each of the first and second body regions between the corresponding source and JFET regions.

6. The MOSFET of claim **4** further comprising:

a first gate extending over but being insulated from the first body region and overlapping each of the first source region and the WET region such that a first channel region is formed along a surface of the first body region between the first source region and the JFET region; and

a second gate extending over but being insulated from the second body region and overlapping each of the second source region and the JEET region such that a second channel region is formed along a surface of the second body region between the second source region and the JFET region regions.

7. The MOSFET of claim **4** further comprising a second semiconductor region of the same conductivity type as the first semiconductor region, the first semiconductor region being over and in contact with the second semiconductor region, the second semiconductor region forming a drain contact region.

8. The MOSFET of claim **1** wherein the first trench region is filled with insulating material.

9. The MOSFET of claim **1** further comprising:

a second trench region extending from the first surface into the first semiconductor region, the second trench region being laterally spaced from the first trench region to form a drift region therebetween, the first and second trench regions being substantially filled with insulation material; and

a second plurality of floating regions along an outer sidewall of the second trench region.

10. The MOSFET of claim **9** wherein a volume of each of the first and second trench regions is greater than one-quarter of the volume of the drift region.

11. The MOSFET of claim **9** wherein a combined width of the first trench region and one of the first plurality of floating regions is greater than one-quarter of a distance between adjacent ones of the first and second plurality of floating regions.

12. A MOSFET comprising:

a first semiconductor region having a first surface;

a first trench region extending from the first surface into the first semiconductor region;

a first plurality of regions along a sidewall of the first trench region; first and second body regions each